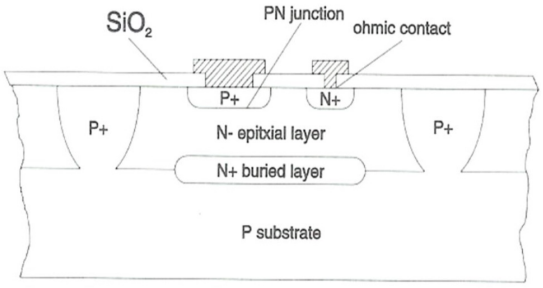
Diodes

PN junction & MN schottky diodes

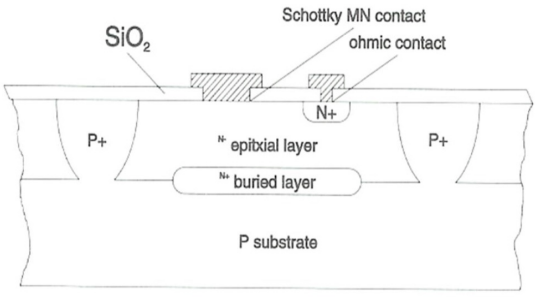
FIGURE 2.1 Diode Symbols: (a) PN junction diode, (b) MN Schottky barrier diode

* Diodes are used in bipolar IC families as actual circuit components
* Diodes are used as clamping diodes at logic circuits inputs
* Clamping diodes purpose is to reduce transient voltages that result from switching transitions
* clamping diodes do not affect normal circuit operation.

Cross sections for digital IC PN & MN diodes



PN junction diodes



MN schottky diode

* schottky diodes are better than PN junctions diodes in terms of high frequency signal.
* PN junctions diodes are better than schottky diodes in terms of reverse bias current.

Diode Modelling

Shockley's Current-Voltage Expression

$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right) \quad \rightarrow \text{Shockley's equation}$$

$I_S \equiv$ reverse saturation current [A]
$\phi_T \equiv$ thermal voltage [V]

$$\phi_T = \frac{kT}{q}$$

$k \equiv$ Boltzmann's constant $= 1.34 \times 10^{-23}$ J/°K
$T \equiv$ temperature [°K]
$q \equiv$ elementary electronic charge $= 1.6 \times 10^{-19}$ C

* The reverse saturation current is the leakage current that flows through a reverse biased diode and is typically $\leq$ pA for PN junction diodes & $\leq$ MA for MN schottky diodes.

Shockley Equation at room temperature.

$T = 27°C$ or $300°K$

$$\phi_T(300°k) = \frac{(1.34 \times 10^{-23})(300)}{(1.6 \times 10^{-19})} = 25.9\,mV$$

$$e^{V/\phi_T} \simeq 40$$

$$I_D(T = 300°K) = I_S\left(e^{40V_D} - 1\right)$$

* Note that this equation is valid only at room temperature.

Example 2.1 ***Relative Forward-Biased PN Junction Diode Current Magnitudes***

Use Shockley's expression to determine the diode current for V_D = 0.1, 0.2, 0.5, 0.7, 0.8, 1, and 2.3 V. Use $I_S = 10^{-14}$ A and assume room temperature.

$I_S = 10^{-14}$ $\quad T = 300°K$

At room temperature $I_D(T = 300°k) = I_S\left(e^{40V_D} - 1\right)$

$I_D(V_D = 0.1) = (10^{-14})\left(e^{40(0.1)} - 1\right) = 536\,fA$

$I_D(V_D = 0.2) = (10^{-14})\left(e^{40(0.2)} - 1\right) = 29.8\,pA$

$I_D(V_D = 0.5) = (10^{-14})(e^{40(0.5)} - 1) = 4.85\,\mu A$

$I_D(V_D = 0.7) = (10^{-14})(e^{40(0.7)} - 1) = 14.5\,mA$

$I_D(V_D = 0.8) = (10^{-14})(e^{40(0.8)} - 1) = 790\,mA$

$I_D(V_D = 1) = (10^{-14})(e^{40(1)} - 1) = 2.35\,kA$

$I_D(V_D = 2.3) = (10^{-14})(e^{40(2.3)} - 1) = 9.02 \times 10^{25}\,A$

Note that for $V_D = 2.3V$ the diode current is an unprecedented $9.02 \times 10^{25}\,A$ & $I_D V_D$ power dissipated in the diode exceeds the entire power output of our sun!

* Note the diode current's exponential dependence on V_D and:
for $V_D = 0.5\,V \Rightarrow I_D$ reaches few μAmps
for $V_D = 0.7\,V \Rightarrow I_D$ reaches mAmps
for $V_D = 0.8\,V \Rightarrow I_D$ reaches hundreds of mAmps
for $V_D = 1V \Rightarrow I_D$ magnitude is at a normally unobtainable hundreds of amps
for $V_D = 2.3V \Rightarrow I_D$ is unprecedented $9.02 \times 10^{25}\,A$
therfore Power dissipated in the diode $I_D V_D$ exceeds the entire output power of our sun.

Example 2.2 ***Relative Reverse-Biased PN Junction Diode Current Magnitudes***

Use Shockley's expression to determine the diode current for $V_D = -1, -10, -100$, and -200 mV. As in Example 2.1 use $I_S = 10^{-14}$ A and assume room temperature.

$I_S = 10^{-14}\,A$, $T = 300^\circ K$

$I_D(T = 300^\circ K) = I_S(e^{40V_D} - 1)$

$I_D(V_D = -1mV) = (10^{-14})(e^{(40)(-1m)} - 1) = -392 \times 10^{-18} = -392\,aA$ (a = atto)

$I_D(V_D = -10mV) = (10^{-14})(e^{(40)(-10m)} - 1) = -3.3\,fA$

$I_D(V_D = -100mV) = (10^{-14})(e^{(40)(-100m)} - 1) = -9.82\,fA$

$I_D(V_D = -200mV) = (10^{-14})(e^{(40)(-200m)} - 1) = -10\,fA = -10^{-14}\,A$

As seen at $V_D \leq -0.2V$ the reverse diode current has a magnitude equal to I_S.

$I_S \equiv$ reverse saturation current.

Note:

$\because e^{x} >> 1 \quad \therefore \quad I_D (V_D > 0.1) \approx I_S e^{V_D/\phi_T}$

$\because e^{x} << 1 \quad \therefore \quad I_D (V_D < -0.1) \approx -I_S$

} (suggested by the two previous examples)

Piecewise Linear Diode Model

* The model has two linear regions

$I_D = 0$ for $V_D \leq V_{D(ON)}$

&

$V_D = V_{D(ON)}$ for $I_D \geq 0$

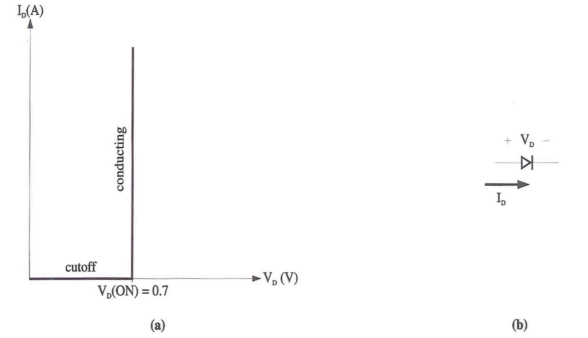


FIGURE 2.3 Piecewise Linear Diode Model: (a) Diode current versus diode voltage, (b) Diode symbol

* for $V_D < V_{D(ON)}$ the diode is cutoff
* for diodes conducting forward currents $V_D = V_{D(ON)}$
* for MN schottky diode $V_{SBD(ON)} = 0.3\,V$ (for silicon)
* Diodes have two modes of operation cutoff & conducting depending on the magnitude & polarity of the diode junction bias V_D.

TABLE 2.1 Diode Modes of Operation

PN Junction Bias	Mode of Operation
Reverse	Cutoff
Forward	Conducting

* The diode breakdown region of operation is avoided in digital circuits & no modeling in this mode is neccessary.

Diode capacitance

* A PN junction diode has a capacitance due to change in depletion region and for forward bias change stored in the semiconductor bulk regions due to injected minority carriers.

* The capacitance must be fully charged to switch the diode into the conducting state and discharge to switch the diode to the cutoff state.

$$C_D(V_D) = \tau_T \frac{I_S}{\phi_T} e^{V_D/\phi_T} + \frac{C_{DO}}{\left(1 - \frac{V_D}{\phi_o}\right)^m}$$

stored minority charge — Depletion region charge.

C_{DO} ≡ zero-bias (i.e $V_D = 0$) junction capacitance [F]

ϕ_o ≡ junction potential (typically 0.7 to 0.9 V) [zero bias]

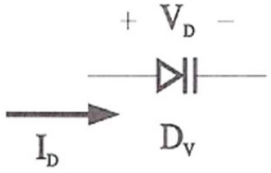
m ≡ grading coefficient ($m \approx 1/2$ or $1/3$ for digital IC diodes)

τ_T ≡ minority carrier ansit time

* The magnitudes of these parameters can be calculated from the diode's physical attributes and fabrication processing parameters such as doping densities.

Varactor Diodes

* forward diode voltage $V_D = -ve$

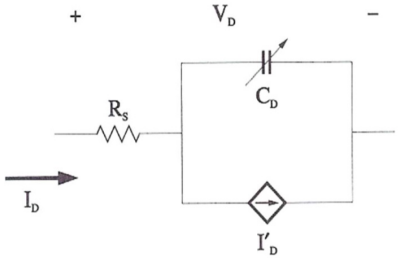


SPICE diode model

SPICE (*Simulation Program with Integrated Circuit Emphasis*)[1][2] is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

https://en.wikipedia.org/wiki/SPICE

* The large signal diode model used in SPICE shown below



SPICE Diode Model

SPICE Diode DC Characteristic

The nonlinear current source I_D' has a value according to the empirically modified Shockley expression

$$I_D' = IS(e^{V_D/N\phi_T} - 1)$$

$N \equiv$ emission coefficient

SPICE Diode Transient Response.

* The transient response of the diode in SPICE is calculated considering the capacitor C_D.

$$C_D = TT\frac{IS}{N\phi_T}e^{V_D/N\phi_T} + \frac{CJO}{\left(1 - \frac{V_D}{VJ}\right)^M}$$

* C_D is equivalently represented as a charge storage element

$$Q_D = TT \times IS(e^{V_D/N\phi_T} - 1) + CJO\int_0^{V_D}\left(1 - \frac{V}{VJ}\right)^{-M} dV$$

* For $V_D > FC\phi_0$

$$C_D = TT\frac{IS}{N\phi_T}e^{V_D/N\phi_T} + \frac{CJO}{\left(1 - \frac{V_D}{VJ}\right)^M} \times \frac{\left[1 - FC(1 + M) + \frac{MV}{\phi_T}\right]}{(1 - FC)^{(1+M)}}$$

TABLE 2.2 SPICE DC Diode Model Parameters

Symbol	Name	Parameter	Units	Default	Typical
I_S	IS	Saturation current	A	1E-14	1E-14
R_S	RS	Parasitic resistance	Ω	0	10
	N	Emission coefficient		1	1

TABLE 2.3 SPICE Transient Diode Model Parameters

Symbol	Name	Parameter	Units	Default	Typical
τ_T	TT	Transit Time	s	0	0.1NS
C_{D0}	CJO	Zero-bias junction capacitance	F	0	2PF
ϕ_0	VJ	Junction potential	V	1	0.8
m	M	Junction grading coefficient		0.5	0.5
	FC	Forward bias depletion capacitance coefficient		0.5	

* For SPICE to calculate transient response one or both of TT & CJO must be specified by the user.

Diode-Resistor Logic (DRL)

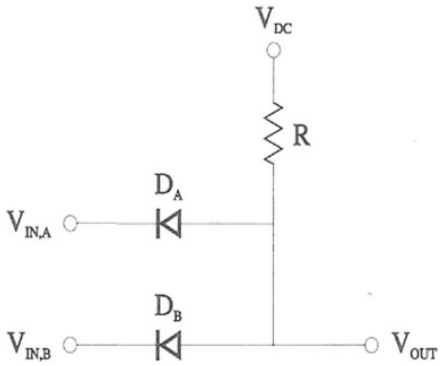
* The two logic functions available with diode-resistor logic are AND gates and OR gates.

Diode AND gate.

① D_I – off

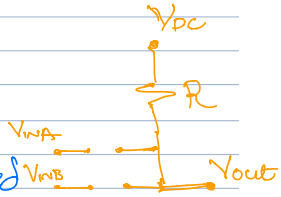
② D_I – ON

③ D_A – off, D_B – ON or vice versa



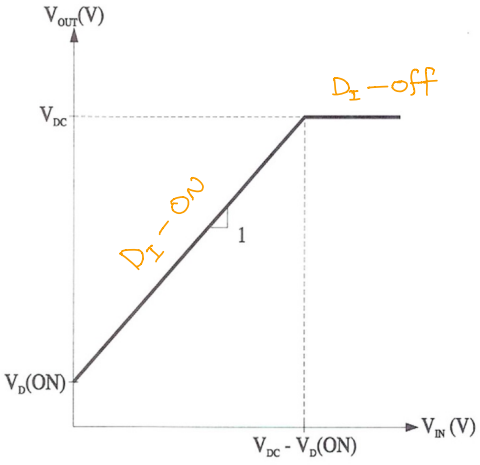
State ①

$V_{out} = V_{DC}$



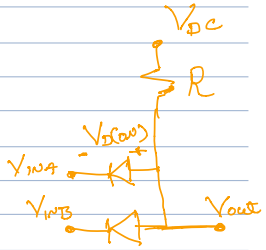
What is the V_{IN} value required for D_I to be off.

$V_{IN} > V_{DC} - V_{D(ON)}$



State ②

$V_{out} = V_{D(ON)} + V_{IN}$

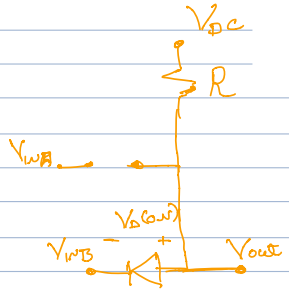


What is the V_{IN} value required for D_I to be ON.

$V_{IN} \leq V_{DC} - V_{D(ON)}$

State ③

$V_{out} = V_{IN} + V_{D(ON)}$

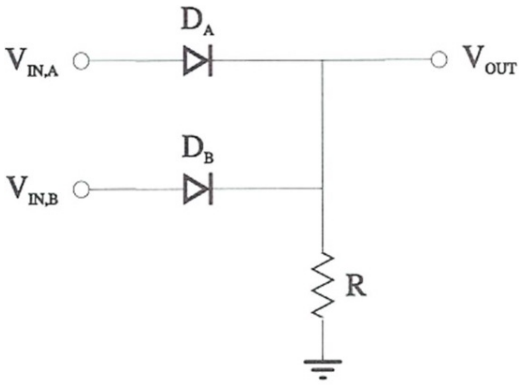


By looking to the possible states of V_{INA}, V_{INB} & V_{out} we can ensure that this DRL gate is an AND gate

V_{INA}	V_{INB}	V_{out}
high	high	high
high	low	low
low	high	low
low	low	low

By looking to the table we can see that this gate is AND Gate.

Diode OR gate

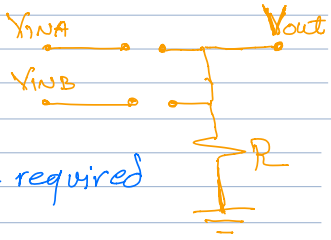


① D_I – off

② D_I – ON

③ D_A – ON, D_B – off or vice versa

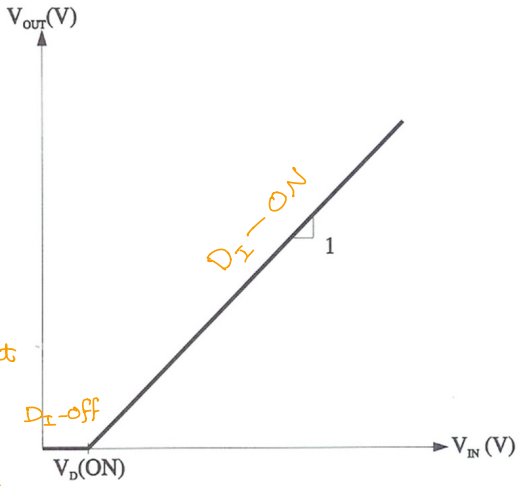
State ①



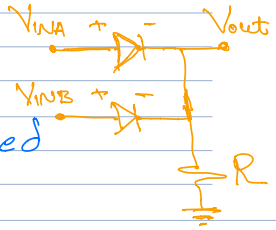
$V_{out} = 0V$

What is the V_{IN} value required for D_I to be off.

$V_{IN} < V_D(ON)$



State ②

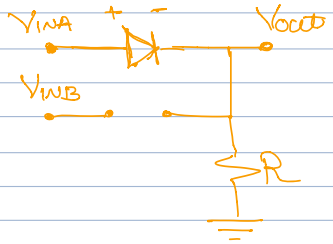


$V_{out} = V_{IN} - V_D(ON)$

What is the V_{IN} value required for D_I to be ON.

$V_{IN} \geq V_D(ON)$

State ③



$V_{out} = V_{IN} - V_D(ON)$

Example 2.3 ***Diode-Resistor AND Gate***

For the two-input diode-resistor AND gate of Figure 2.6, show that if V_{INA} is 1 V above V_{INB}, D_A is cutoff.

$V_{INA} = V_{INB} + 1$ ——— (1)

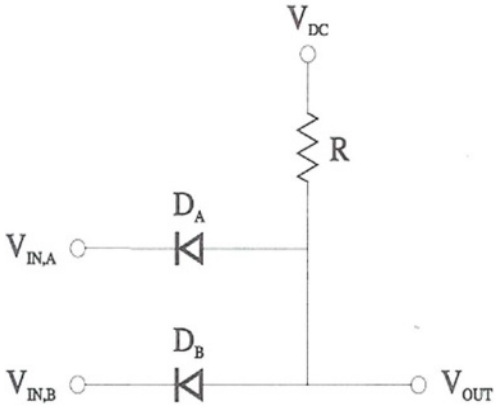
$V_{DA} = V_{out} - V_{INA}$ ——— (2)

$V_{DB} = V_{out} - V_{INB}$ ——— (3)

We assume that D_A is conducting (ON)

$\therefore V_{DA} = 0.7V$

$V_{out} = V_{INA} + V_{D(ON)} = V_{INA} + 0.7$ ——— (4)



by substitute (4) in (3)

$V_{DB} = (V_{INA} + 0.7) - V_{INB}$ ⇒ by substitute (1) in this equation

$V_{DB} = (V_{INB} + 1) + 0.7 - V_{INB} = 1.7V$

But It's not possible for V_{DB} to be 1.7V therefore D_A is not conducting

$\therefore D_A$ is cutoff , D_B is ON

$V_{out} = V_{INB} + 0.7$ ——— (5)

by subtitute (5) in (2)

$V_{DA} = V_{out} - V_{INA} = (V_{INB} + 0.7) - V_{INA} = V_{INB} - V_{INA} - 0.7 = -1 + 0.7 = -0.3V$

$\therefore V_{DA} < V_{D(ON)}$

$\therefore D_A$ is cutoff

Diode logic: "IN" or "OUT"

IN ≡ OR

AND ≡ OUT

* Note that OUT & AND have three letters while IN & OR have two letters, This way you can remember that IN ≡ OR & AND ≡ OUT.

Level shifted diode-resistor logic.

* Voltage degradation. is the offset from the origin with the output and input voltages never zero together.

* Voltage degradation is a reduction or increase in the output voltage level by one diode drop [$V_{D(ON)}$].

* Level shifting diode is a diode included at the output of DRL for voltage degradation correction.

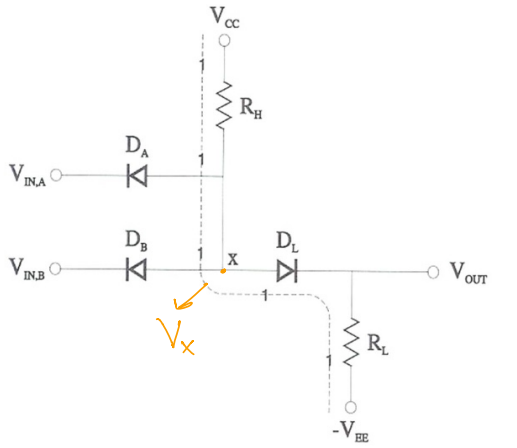
Level-shifted AND Gate

① D_I — ON , D_L — ON

② D_I — ON , D_L — off

③ D_I — off , D_L — ON

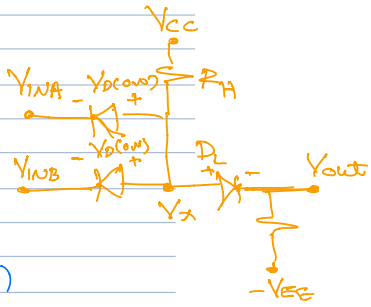
④ D_I — off , D_L — off



State ①

$V_X = V_{IN} + V_{D(ON)}$ ——— ①

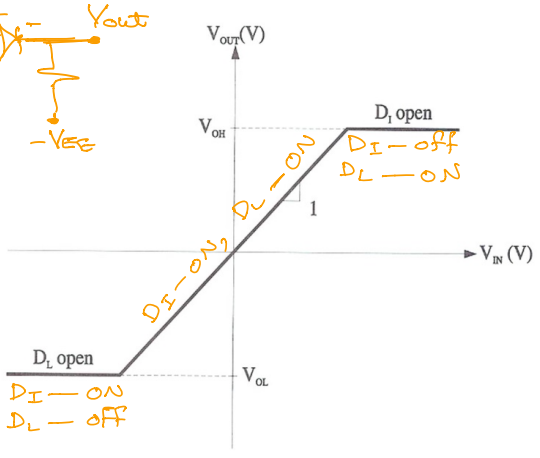
$V_{out} = V_X - V_{D(ON)}$ ——— ②



By subtitute ① in ②

$V_{out} = V_{IN} + V_{D(ON)} - V_{D(ON)}$

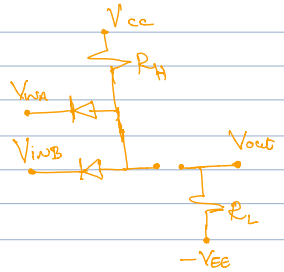
$V_{out} = V_{IN}$



State ②

$V_{out} = -V_{EE} = V_{OL}$

$V_{IN} \leq -V_{EE}$



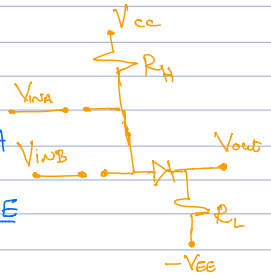
State ③

$V_{out} = V_{CC} - IR_H - V_{D(ON)}$

or

$V_{out} = IR_L - V_{EE} = V_{OH}$

$I = \dfrac{V_{CC} - V_{D(ON)} + V_{EE}}{R_H + R_L}$



* Since V_{OH} depends on R_H & R_L therefore chosing R_H & R_L value is a matter of design and it will specify V_{OH} value

State ④

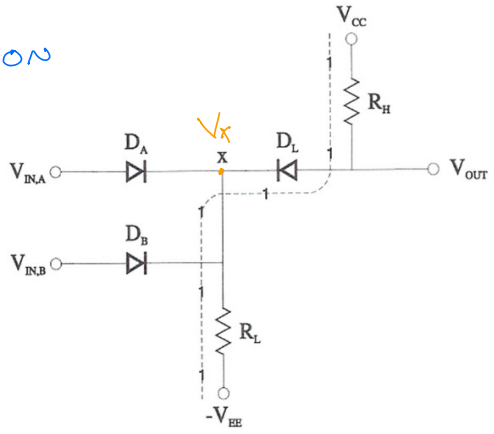
* the required conditions for D_I & D_L both to be off is not possible to achieve therefore there is

no state ④ for this gate circuit

Level-Shifted OR Gate

① D_I – ON, D_L – ON ② D_I – off, D_L – ON

③ D_I – ON, D_L – off



State ①

$V_{out} = V_x + V_{D(ON)}$

$V_x = V_{IN} - V_{D(ON)}$

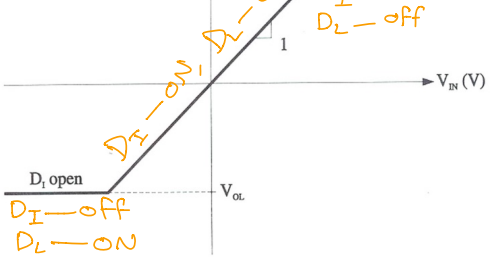
$V_{out} = V_{IN} - V_{D(ON)} + V_{D(ON)} = V_{IN}$

State ②

$V_{out} = V_{CC} - IR_H$

$= -V_{EE} + IR_L + V_{D(ON)} = V_{OL}$

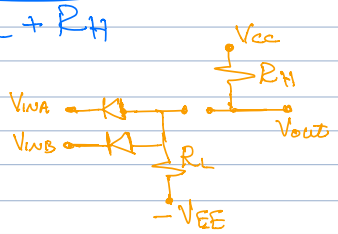
$I = \dfrac{V_{CC} - V_{D(ON)} + V_{EE}}{R_L + R_H}$



State ③

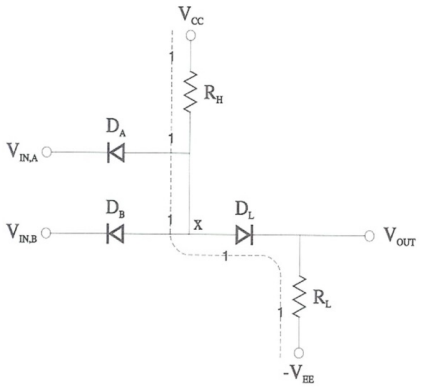
$V_{out} = V_{CC}$

$V_{out} = V_{OH}$



Example 2.4 ***Level-Shifted Diode-Resistor AND Gate***

Find the output low and high voltages for the level shifted diode-resistor AND gate shown in Figure 2.8a. Use $V_{CC} = 4$ V, $-V_{EE} = -4$ V, $V_D(ON) = 0.7$ V, $R_H = 1$ kΩ, and $R_L = 2$ kΩ.



$V_{CC} = 4V$, $V_{EE} = 4V$, $V_{D(ON)} = 0.7V$

$R_H = 1k\Omega$, $R_L = 2k\Omega$

$V_{OL} = -V_{EE} = -4V$

$V_{OH} = IR_L - V_{EE} = V_{CC} - IR_H - V_{D(ON)}$

$I = ?$

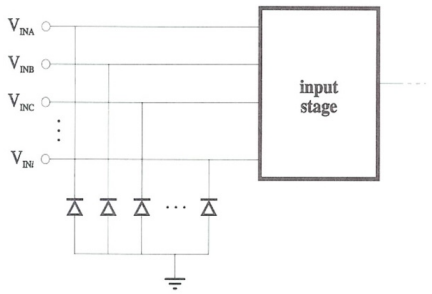
$I = \dfrac{V_{CC} - V_{D(ON)} + V_{EE}}{R_H + R_L} = \dfrac{4 - 0.7 + 4}{3K} = 2.43mA$

$V_{OH} = IR_L - V_{EE} = 2.43m \times 2K - 4 = 0.87V$

Clamping Diodes

* When input to a gate is switched high to low the input voltage sometimes swings beyond 0V. this called ringing and may cause physical damage to the gate itself.

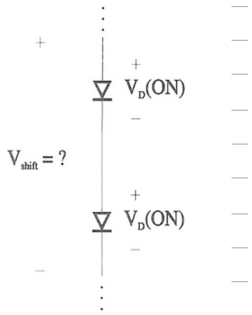
* Connecting diodes to each input of a gate reduces these problems by preventing the inputs from falling below one diode drop of -0.7V



Level-Shifting Diodes

* it used to level shift the output voltage.

* another use of diode forward voltage is to ensure that sub-circuits with complementary objectives are not conducting simultaneously.



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